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EXAMINER

ALI, SYED J

ART UNIT PAPER NUMBER

2127

DATE MAILED: 05/12/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/534,191

Applicant(s)

LEE ET AL.

Examiner

Syed J Ali

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3, 5-9.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3, 7, and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3, 7, and 25 contain grammatical errors rendering the claims indefinite.

Claim Objections

3. Claims 5, 14, and 23 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 5 recites a similar limitation as claimed in parent claim 3. Specifically, the identification of a further way within the selected set of memory as the candidate way is essentially the same as identification of a further location as the candidate location.

Claims 14 and 23 are objected to for similar reasons.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-5, 11-14, 21-23, and 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Sturges et al. (USPN 6,295,580) (hereinafter Sturges).

As per claim 1, Sturges discloses a method including:

dedicating a first portion of a resource exclusively to a first thread (col. 9 lines 15-22, “the processes are mapped to disjoint data cache partitions. This effectively gives each process its own private data cache”);

dedicating a second portion of the resource exclusively to a second thread (see above citation); and

dynamically sharing a third portion of the resource between the first and second threads (col. 8 line 61 – col. 9 line 14, “the cache partition indicators...allocate banks B1 and B2 to the processes P3 and P4”, wherein the indicators tell the system that both P3 and P4 are allowed to use the data cache).

As per claim 2, Sturges discloses the method of claim 1 wherein the dynamic sharing of the third portion of the resource is performed according to resource demands of the respective first and second threads (col. 8 line 61 – col. 9 line 14, “when the processor is expecting to execute the process P3, it now has a cache facility”, wherein based on the data caching needs of whichever processes are sharing the partition, the cache facility operates accordingly).

As per claim 3, Sturges discloses the method of claim 1 wherein the resource comprises a memory resource including first and second portions dedicated to the first and second threads respectively and a third portion shared between the first and second threads, the method including:

identifying a first location within the memory resource as a candidate location to receive an information item associated with the first thread (col. 7 lines 29-45, “The partition indicator gives information regarding the partition into which the data item may be placed”);

determining whether the candidate location is within the first or the third portion of the memory resource dedicated to the first thread (col. 7 lines 29-45, “The value of 1 in bit j of the partition indicator means that the data may not be placed in partition j. The value of 0 in bit j means that the data may be placed in partition j”);

if the candidate location is within the first or the third portion of the memory resource, then storing the information associated the first thread at the candidate location (col. 7 lines 29-45, wherein once a determination is made as to where the data can be placed, the data is stored in the corresponding cache partition); and

if the candidate location is within the second portion of the memory resource then identifying a further location as being the candidate location (col. 7 line 61 – col. 8 line 4, “The decision circuit 52 determines the proper partition of the cache into which data...is to be located”).

As per claim 4, Sturges discloses the method of claim 3 wherein the memory resource comprise a N way set associative memory and wherein the first portion comprises a first way dedicated to the first thread (col. 7 lines 49-55, “the partitions would behave as a k-way set associative cache, where k partitions are allocated to a task”), the second portion comprises a second way dedicated to the second thread and the third portion comprises a third way shared between the first and second threads (see citation in claim 1 for how the cache is divided among tasks), wherein the identification of the first location as the candidate location comprises identifying a selected way within a selected set of the memory as a candidate way to receive the information item associated with the first thread (col. 7 lines 29-48, “The partition indicator gives information regarding the partition into which the data item may be placed”).

As per claim 5, Sturges discloses the method of claim 4 wherein the identification of the further location as the candidate location comprises identifying a further way within the selected

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set of the memory as the candidate way to receive the information item associated with the first thread (col. 7 line 61 – col. 8 line 4, “The decision circuit 52 determines the proper partition of the cache into which data...is to be located”).

As per claim 11, it is rejected for similar reasons as stated for claim 1 above. Further, as Sturges is applied to concurrent processes, it is well known that one way of implementing concurrent processes is through multithreading. This is discussed within Sturges as well (col. 6 lines 1-44).

As per claims 12-14, they are rejected for similar reasons as stated for claims 3-5 above.

As per claims 21-23, they are rejected for similar reasons as stated for claims 3-5 above.

As per claims 29-30, they are rejected for similar reasons as stated for claims 1-2 above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6-9, 15-19, and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sturges in view of Witt (USPN 6,161,167).

As per claim 6, Sturges does not specifically disclose the method of claim 4 wherein the identification of the selected way within the selected set as the candidate way comprises identifying a way within the select set that was least recently used.

Witt discloses the method of claim 4 wherein the identification of the selected way within the selected set as the candidate way comprises identifying a way within the select set that was least recently used (col. 13 lines 27-46, "Tag control unit 52 selects an LRU group from which to select the tag storage location, and then selects the tag storage location within the selected LRU group which is storing the least recently used cache line").

It would have been obvious to one of ordinary skill in the art to combine Sturges with Witt since Sturges does not specifically provide a solution for how to handle a case in which the destination block is one that is not accessible by the particular thread. Therefore, to utilize the method of Witt and store the data in the least recently used cache line allows data to be accessed faster, while minimizing the likelihood of replacing important data, since the data has not been accessed for some time.

As per claim 7, the modified Sturges does not specifically disclose the method of claim 5 wherein the identification of the further way within the selected set a candidate way comprises identifying a way within the selected set that was second-least recently used. However, "Official Notice" is taken that to do so would have been obvious to one of ordinary skill in the art.

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Specifically, in the instance that the least recently used cache block remains within the partition that is inaccessible to the thread in question, a mechanism must be in place to find a suitable cache block for that data. Since the intention of using the least recently used block was to minimize the chances that data that will need to be accessed again is replaced, it would have been obvious to attempt to replace the next least recently used block, as claimed. Further, Witt does disclose a way of identifying which cache block was second least recently used, third least recently used, etc. (col. 12 line 66 – col. 13 line 20, “The binary value ‘00’ may comprise the least recently used of the entries within the LRU group. Similarly, the binary value ‘01’ may comprise the second least recently used of the entries”).

As per claim 8, Witt discloses the method of claim 6 including examining a Least Recently Used (LRU) history for the selected set to identify the way that was least recently used (col. 12 line 66 – col. 13 line 20, wherein each cache partition or block has an identifier associated with it that identifies how recently the cache block was used in relation to the other blocks).

As per claim 9, Witt discloses the method of claim 8 including examining a set of entries within the LRU history for the selected set, each entry within the set of entries indicating a respective way within the selected set, wherein the set of entries is ordered in a sequence determined by least recent usage of a respective way and the selection of the candidate way comprises performing a sequential examination of the entries of the set of entries to locate a least recently used way that comprises either the first or the second way (col. 12 line 66 – col. 13 line

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20, wherein the cache lines are numbered in such a way indicative of which cache line was least recently used, second least recently used, etc.)

As per claim 15, it is rejected for similar reasons as stated for claim 6 above. Specifically, concessions have to be made in the case where data is to be cached in a partition in which the thread is not allowed to write.

As per claim 16-19, it is rejected for similar reasons as stated for claim 6-9 above.

As per claim 24, it is rejected for similar reasons as stated for claims 1 and 8 above.

As per claim 25, the discussion of claim 7 provides motivation for why the second portion should be excluded from consideration regarding the least recently used history. Therefore, the discussion of claim 7 also forms the basis for rejection of the present claim.

As per claim 26, it is rejected for similar reasons as stated for claim 4 above.

As per claim 27, it is rejected for similar reasons as stated for claim 8 above.

5. Claims 10, 20, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sturges in view of Witt, and further in view of Sager (USPN 6,542,921).

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As per claim 10, the modified Sturges does not specifically disclose the method of claim 9, wherein memory comprises a trace cache memory, and wherein the information item associated with the first thread comprises a microinstruction of the first thread.

Sager discloses a system wherein memory comprises a trace cache memory, and wherein the information item associated with the first thread comprises a microinstruction of the first thread (col. 5 lines 20-42, "The trace delivery engine 230 functions as a microinstruction cache and...includes a trace cache 232).

It would have been obvious to one of ordinary skill in the art to combine the modified Sturges with Sager, since Sager describes an additional system on which the method of Sturges could be applied. Although Sturges refers to partitioning of caches in general, it would have been a simple modification to apply the same method to a trace cache.

As per claim 20, it is rejected for similar reasons as stated for claim 10 above.

As per claim 28, it is rejected for similar reasons as stated for claim 10 above.

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Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (703) 305-8106. The examiner can normally be reached on Mon-Fri 8-5:30, 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (703) 305-8498. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



Syed Ali
April 21, 2003

MAJID BANANKHAH
PRIMARY EXAMINER